L Number	Hits	Search Text	DB	Time stamp
•	1	5437034.pn.	USPAT	2003/12/30 13:01
-	1	6226776.pn.	USPAT	2003/12/19 17:30
-	1	5600579.pn.	USPAT	2003/12/19 17:30
-	1	5774380.pn.	USPAT	2003/12/19 17:31
-	11	("5437034" US-6226776 US-5600579 US-5774380) and (HDL	USPAT	2003/12/27 22:37
		VHDL system simulation simulating simulate circuit model code		
		coded coding storing store stored saved save saving recording		
		record recorded executed hardware description language object code "C" programming program programmed)		
	208	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/03 18:59
	200	(simulation simulating simulate) and circuit and model and (code	OSFAT	200-1/01/03 10.39
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed)		
_	74	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/27 22:40
	• •	(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and @pd < "19990930"		
-	74	(HDL VHDL "hardware description language") and system and	USPAT;	2003/12/27 22:40
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930"	IBM_TDB	
-	62	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:42
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
	<b>50</b>	(convert converting converted compile compiling compiled)	LICDAT.	2002/12/27 22:42
-	58	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code	USPAT; US-PGPUB;	2003/12/27 22:43
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and	1011_100	
		(clock clocking clocked cycle cycling)		
_	49	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:44
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	-555, -2, -2
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling)	Ì	
-	49	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:45
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated)		
_	49		USPAT;	2003/12/31 00:08
-	75	(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	2003/12/31 00.00
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated) and object		

-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:49
-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/27 22:54
-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/27 22:55
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/28 21:46
-	4	(US-5600579-\$ or US-5437034-\$ or US-6226776-\$ or	USPAT	2003/12/27 22:59
-	2	US-5774380-\$).did. "60156732" "60/156,732" "60,156,732"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 23:00
-	0 58	("convert" "compile") adj "HDL" adj "to" adj "binary" ("convert" "compile") adj "HDL"	USPAT USPAT	2003/12/28 21:10 2003/12/28 21:10
-	0	("convert" "compile") adj "HDL" same "binary"	USPAT	2003/12/28 21:10
-	22 18	("convert" "compile") adj "HDL" same code ("convert" "compile") adj "HDL" same code and @ad <	USPAT USPAT	2003/12/28 21:11 2003/12/28 21:37
-	0	"19990930" ("convert" "compile") adj "HDL" same binary and @pd <	USPAT	2003/12/28 21:38
-	0	"19990930" ("convert" "compile") adj "HDL" same binary and @ad <	USPAT	2003/12/28 21:38
-	2	"19990930" ("convert" "compile") adj "HDL" same machine and @ad <	USPAT	2003/12/28 21:45
		"19990930"		

-	1	("convert" "compile") adj "HDL" same machine and @pd < "19990930"	USPAT	2003/12/28 21:45
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:47
-	9	interface") (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) same (machine code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:55
-	4	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) adj4 (code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 22:08
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:56
-	1	compiled compiler compilers) and (code binary assembly machine) (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19980930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:57
-	0	compiled compiler compilers) and (code binary assembly machine) (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and 5437037.pn.	USPAT	2003/12/30 13:02

-	0	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/30 13:03
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and executed and object and "C" and		
		(programming program programmed) and 5437037.pn.		
	اما		LICDAT	2002/12/20 12 02
-	0	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/30 13:03
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and "C" and (programming program programmed)		
		and 5437037.pn.		
i _	1	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/31 00:33
		(simulation simulating simulate) and circuit and model and	00.711	2003, 12, 31 00.33
		(programming program programmed) and 5437037.pn.		
-	28	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/31 00:09
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	ŀ
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19980930" and	IBM_TDB	
1		(convert converting converted compile compiling compiled) and	1011_100	
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated) and object		
-	17	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/31 00:09
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
			DERWENT;	
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and @pd < "19980930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated) and object and oriented		
_	0	(HDL VHDL "hardware description language" ) near4 (compile	USPAT	2003/12/31 00:35
	_	compiled compiling convert converting converted convertion)		, , , , , , , , , , , , , , , , , , , ,
		near4 (assembly assembling assembled)		
<u> </u>	13	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:36
-	13		USFAI	2003/12/31 00.30
1		compiled compiling convert converting converted convertion)		
•		same (assembly assembled)		2002/42/24 22 25
-	13	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:36
		compiled compiling convert converting converted convertion)		
		same (assembly assembling assembled) and pd<19980930		
_	1	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:40
	_	compiled compiling convert converting converted convertion)		, , , ,
		same (assembly assembling assembled) and @pd<19980930		
	٦	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:44
-	2		USFAI	2003/12/31 00.44
		compiled compiling convert converting converted convertion)		
		same (assembly assemling assembled) and @pd<19990930		
-	4	((HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 12:40
		compiled compiling convert converting converted convertion)		
		same (binary assembly assembling assembled) and		
		@pd<19990930) and (HDL VHDL hardware description language		
		compile compiling compiled compilation converting convert		
1	300	converted convertion binary assembling assembly)	LICDAT	2002/12/21 12 10
-	380	"HDL" and "RTL"	USPAT	2003/12/31 12:40
-	306	"HDL" same "RTL"	USPAT	2003/12/31 12:40
-	141	"HDL" same "RTL" and ("binary" "assembly")	USPAT	2003/12/31 12:41
-	123	"HDL" same "RTL" and ("binary" "assembly") and interface	USPAT	2003/12/31 12:41
-	13	"HDL" same "RTL" and ("binary" "assembly") and interface and	USPAT	2003/12/31 13:50
		@pd< "19980930"		, -=,
_	9538	Meyer.in.	USPAT	2003/12/31 13:51
_	_			
-	0	Stven adj4 Meyer	USPAT	2003/12/31 13:51
-	1 1	Steven adj4 Meyer	USPAT	2003/12/31 13:51
-	147	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/07 12:28
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$		
	<b>-</b>	The same bearing bearing by and brockers	<del></del>	<u></u>

- 106 (HDL VHDL "hardware description language" ) and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur\$ and task\$ and block\$ and delay\$  - 106 (HDL VHDL "hardware description language" ) and system and USPAT	2004/01/03 19:03
coded coding) and (storing store stored saved save saving recording recorded) and executed and object and "C" and (programming program programmed) and procedur\$ and task\$ and block\$ and delay\$  - 106 (HDL VHDL "hardware description language" ) and system and USPAT	
recording record recorded) and executed and object and "C" and (programming program programmed) and procedur\$ and task\$ and block\$ and delay\$  - 106 (HDL VHDL "hardware description language" ) and system and USPAT	
(programming program programmed) and procedur\$ and task\$ and block\$ and delay\$ - 106 (HDL VHDL "hardware description language" ) and system and USPAT	
and block\$ and delay\$ - 106 (HDL VHDL "hardware description language" ) and system and USPAT	
- 106 (HDL VHDL "hardware description language" ) and system and USPAT	
	2004/01/03 20:13
(simulation simulating simulate) and circuit and model and (code	
coded coding) and (storing store stored saved save saving	
recording record recorded) and executed and object and "C" and	
(programming program programmed) and procedur\$ and task\$	
and block\$ and delay\$ and control\$ and (operation process)	
- 22 (HDL VHDL "hardware description language" ) and system and USPAT	2004/01/03 20:24
(simulation simulating simulate) and circuit and model and (code	
coded coding) and (storing store stored saved save saving	
recording record recorded) and executed and object and "C" and	
(programming program programmed) and procedur\$ and task\$	
and block\$ and delay\$ and control\$ and (operation process) and	
@pd<19980930	
- 92 (HDL VHDL "hardware discription language" Verilog) and (PLI USPAT;	2004/01/06 14:36
"programming language interface") US-PGPUB	
EPO; JPO;	
DERWENT	
IBM_TDB	
- 6 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/07 12:29
language" Verilog) and (PLI "programming language interface") US-PGPUB	
EPO; JPO;	
DERWENT	
IBM_TDB	
- 5 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 14:40
language" Verilog) and (PLI "programming language interface") US-PGPUB	
and (C++ "C" "object-oriented language" "object oriented") EPO; JPO;	
DERWENT	
IBM_TDB	
- 4 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 14:41
language" Verilog) and (PLI "programming language interface") US-PGPUB	
and (C++ "C" "object-oriented language" "object oriented") and EPO; JPO;	
(simulation simulated simulate simulating) and (binary object code   DERWENT	
assembly) IBM_TDB	
- 1 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 14:42
language" Verilog) and (PLI "programming language interface") US-PGPUB	
and (C++ "C" "object-oriented language" "object oriented") and EPO; JPO;	
(simulation simulated simulate simulating) and (binary assembly) DERWENT	
and (object code) IBM_TDB	
- 1 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 14:43
language" Verilog) and (PLI "programming language interface") US-PGPUB	
and (C++ "C" "object-oriented language" "object oriented") and EPO; JPO;	
(simulation simulated simulate simulating) and (binary assembly) DERWENT	
IBM_TDB	
- 1 @pd < "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 14:43
language" Verilog) and (PLI "programming language interface") US-PGPUB	
and (C++ "C" "object-oriented language" "object oriented") and EPO; JPO;	
(simulation simulated simulate simulating) and (binary assembly) DERWENT	,
and (memory stored storing storage) IBM_TDB	
- 0 @pd`< "19980930" and (HDL VHDL "hardware discription USPAT;	2004/01/06 16:06
language" Verilog) and (PLI "programming language interface") US-PGPUB	
EPO; JPO;	
DERWENT	,
IBM_TDB	

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	22	(UDL VUIDL "handware description language" \ and sistem and	USPAT	2004/01/07 12:20
-	22	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code	USPAT	2004/01/07 12:29
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$ and		
		(simulat\$ same binary)		
_	1	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/07 12:50
	_	language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		and (simulat\$ same binary)	EPO; JPO;	
		, , , , , , , , , , , , , , , , , , , ,	DERWENT;	
			IBM_TDB	
_	0	(binary assembly) same "all simulator"	USPAT;	2004/01/07 12:52
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
		(hinan canadah ) asas Ilali aimulakandi	IBM_TDB	2004/01/07 12:52
-	0	(binary assembly) same "all simulators"	USPAT;	2004/01/07 12:52
			US-PGPUB; EPO; JPO;	
			DERWENT;	
			IBM_TDB	
_	0	(binary assembly) and "all simulators"	USPAT;	2004/01/07 12:52
			US-PGPUB;	, , ,
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	6653	(binary assembly) and simulator	USPAT;	2004/01/07 12:52
			US-PGPUB;	:
			EPO; JPO;	
			DERWENT;	
	3378	(binary assembly) and simulator and @pd < "19980930"	IBM_TDB USPAT;	2004/01/07 12:53
-	3376	(billary assembly) and simulator and wpd < 19900930	US-PGPUB;	2004/01/07 12.55
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(binary assembly) and simulator and @pd < "19980930" and	USPAT;	2004/01/07 12:54
		703/*.ccls	US-PGPUB;	
			EPO; JPO;	
		, i	DERWENT;	
	225	(hinama accomple) and simulator and @nd a #40000000" and	IBM_TDB	2004/01/07 12:54
-	335	(binary assembly) and simulator and @pd < "19980930" and "703"	USPAT; US-PGPUB;	2004/01/07 12:54
		/03	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(binary assembly) and simulator and @pd < "19980930" and	USPAT;	2004/01/07 12:55
		"703" and "all"	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1	(binary assembly) and simulator and @pd < "19980930" and "all"	USPAT;	2004/01/07 12:55
			US-PGPUB;	
			EPO; JPO; DERWENT;	
			IBM_TDB	
	L		םם ו_וחד	L